

C L A I M S

1. A polishing pad used for polishing a semiconductor wafer in a mirror polishing process, characterized in that a content of zinc compounds included in the polishing pad is 200ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.
2. A polishing pad used for polishing a semiconductor wafer in a finish polishing process, characterized in that a content of zinc compounds included in the polishing pad is 100ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.
3. A polishing pad used for polishing a semiconductor wafer in a finish polishing, characterized in that the polishing pad does not include zinc compounds.
4. The polishing pad used for polishing a semiconductor wafer according to any one of Claims 1 - 3, characterized by comprising a base layer formed of nonwoven fabric and a porous surface layer.
5. The polishing pad used for polishing a semiconductor wafer according to Claim 4, characterized

in that a content of zinc compounds in the surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.

6. A polishing pad used for polishing a semiconductor in a mirror polishing process, characterized in that it comprises a base layer formed of nonwoven fabric and a porous surface layer, and a content of zinc compounds included in the surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the surface layer.

7. The polishing pad for polishing a semiconductor wafer according to claim 6, characterized in that the surface layer does not include zinc compounds.

8. The polishing pad for a semiconductor wafer according to any one of Claims 4-7, characterized in that the surface layer is foamed of foamed polyurethane.

9. A method for polishing a semiconductor wafer, characterized in that the polishing is performed by using the polishing pad according to any one of claims 1-8.

10. A method for polishing a semiconductor wafer, characterized in that the finish polishing is performed

while a concentration of zinc compounds is kept to
200ppm or less in the position where the semiconductor
wafer is in contact with the polishing pad.

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